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EXAMINER
PETRANEK, JACOB ANDREW

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/748,173	GAT ET AL.
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-8,11-16 and 20-25* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8,11-16 and 20-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-4, 6-8, 11-16, 20-25 are pending.

2.   The office acknowledges the following papers:

Claims and arguments filed on 8/18/2006.

Withdrawn

3.   The 35 USC § 112 second paragraph rejection for claim 5 has been withdrawn

due to amendment.

New Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 1-2, 6-8, 11-12, 15-16, 20 and 23-25 are rejected under 35 U.S.C.

§102(b) as being anticipated by Reinman et al. ("Optimizations Enabled by a Decoupled

Front-End Architecture"), in view of Giacalone et al. (U.S. 6,272,624).

6.   As per claim 1:

Reinman disclosed a method comprising:

Storing said branch predictions in a queue (Reinman: Figure 5, sections 3 and

4.1 and 5.2)(Predictions are stored in the fetch target queue); and

Delivering a stored branch prediction from said queue to an instruction fetch unit

(Reinman: Figure 5, sections 3 and 4.1).

Reinman failed to teach generating branch predictions for two sequential lines in

parallel during a prediction period.

However, Giacalone disclosed generating branch predictions for two sequential

lines in parallel during a prediction period (Giacalone: Figure 3, column 8 lines 47-67

continued to column 9 lines 1-34)(A line is a single instruction. Figure 3 shows multiple

branch instructions being predicted within a single prediction period).

The advantage of using a branch predictor that can predict multiple branch

instructions per cycle is that it's needed to achieve high performance in very wide

superscalar processors (Giacalone: Column 2 lines 26-34). One of ordinary skill in the

art would have been motivated by increased performance in superscalar processors to

add the branch predictor of Giacalone to the processor Reinman. Thus, it would have

been obvious to one of ordinary skill in the art at the time of the invention to implement

the branch predictor of Giacalone to the processor of Reinman for the advantage of

increased performance in a superscalar processor.

7.   As per claim 2:

Reinman and Giacalone disclosed the method as in claim 1, wherein said

prediction period comprises two clock cycles (Giacalone: Figure 3, column 8 lines 47-67

continued to column 9 lines 1-34)(It's obvious to one of ordinary skill in the art that

branch prediction can take more than one cycle depending on the clock speed and the

complexity of the branch predictor. Thus, it's obvious to one of ordinary skill in the art at the time of the invention that the branch predictor could take two cycles.).

8.   As per claim 6:

Reinman and Giacalone disclosed the method as in claim 1.

Reinman and Giacalone failed to teach generating branch predictions for a stream of addresses during a stall of said instruction fetch unit.

However, it would have been obvious to one of ordinary skill in the art that the only time it would have been necessary for the branch predictor to stop generating predictions is when the instruction fetch queue is full. It would have also been obvious to one of ordinary skill in the art that the instruction fetch unit could be stalled on an instruction cache miss while the instruction fetch queue was not full. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the predictor could continue predicting branches while the instruction fetch queue was stalled as long as the instruction fetch queue was not full.

9.   As per claim 7:

Reinman and Giacalone disclosed the method as in claim 1, comprising generating during a cycle a prediction for a line, said line being other than the line being fetched by said instruction fetch unit during said cycle (Reinman: Figure 5, section 4.1)(Figure 5 shows branch predictions being generated and stored in the instruction fetch queue. Thus, the predictor deals with different instructions than the instruction fetch unit during the same cycle.).

10.   As per claim 8:

The specific limitation(s) of claim 8 essentially recite the specific limitation(s) of claim 7. Therefore, claim 8 is rejected for the same reason(s) as claim 7.

11.   As per claim 11:

Reinman and Giacalone disclosed the method as in claim 1, comprising delivering a branch prediction to said instruction fetch unit in the same prediction period as said branch prediction is written to said queue (Reinman: Figure 5, sections 3 and 4.1)(It's obvious to one of ordinary skill in the art at the time of the invention that the queue of figure 5 is capable of adding items and erasing items from the queue in the same cycle.)

12.   As per claim 12:

Claim 12 essentially recites the same limitations of claim 1. Claim 12 additionally recites the following limitations:

A branch prediction unit (Reinman: Figure 5, section 4.1); and

An instruction fetch unit (Reinman: Figure 5, section 4.1).

13.   As per claim 15:

The specific limitation(s) of claim 15 essentially recite the specific limitation(s) of claim 2. Therefore, claim 15 is rejected for the same reason(s) as claim 2.

14.   As per claim 16:

The specific limitation(s) of claim 16 essentially recite the specific limitation(s) of claim 11. Therefore, claim 16 is rejected for the same reason(s) as claim 11.

15.   As per claim 20:

Claim 20 essentially recites the same limitations of claim 12. Claim 20

additionally recites the following limitations:

DRAM (Reinman: Figure 5)(Figure 5 shows a prefetch unit that fetches

instructions from L2 cache or higher memories, such as main memory. Official notice is

taken that the L2 cache or higher memory like main memory could either comprise a

DRAM.).

16.   As per claim 23:

The specific limitation(s) of claim 23 essentially recite the specific limitation(s) of

claim 2. Therefore, claim 23 is rejected for the same reason(s) as claim 2.

17.   As per claim 24:

The specific limitation(s) of claim 24 essentially recite the specific limitation(s) of

claim 11. Therefore, claim 24 is rejected for the same reason(s) as claim 11.

18.   As per claim 25:

The specific limitation(s) of claim 25 essentially recite the specific limitation(s) of

claim 8. Therefore, claim 25 is rejected for the same reason(s) as claim 8.

19.   Claims 3-4, 13-14, and 21-22 are rejected under 35 U.S.C. §103(a) as being

unpatentable over Reinman et al. ("Optimizations Enabled by a Decoupled Front-End

Architecture"), in view of Giacalone et al. (U.S. 6,272,624), further in view of Stiles et al.

(U.S. 5,515,518).

20.   As per claim 3:

Reinman disclosed the method as in claim 1.

Reinman failed to teach segmenting a cache of a branch predictor into a first side and a second side, where entries on said first side correspond to addresses having even-numbered indexes, and entries on said second side correspond to addresses having odd-numbered indexes.

However, Stiles disclosed segmenting a cache of a branch predictor into a first side and a second side, where entries on said first side correspond to addresses having even-numbered indexes, and entries on said second side correspond to addresses having odd-numbered indexes (Stiles: Figure 9 element 155, column 15 lines 51-58)(Stiles disclosed a direct-mapped branch prediction cache. The segmented cache as claimed is a direct-mapped branch prediction cache that is divided into a lower and upper segment that divides odd and even instruction addresses. It would have been obvious to one of ordinary skill in the art at the time of the invention that having a segmented cache has no effect on the accuracy of the branch prediction and is simply slightly reorganizing the layout of the cache. Also, it would have been obvious to one of ordinary skill in the art at the time of the invention that the segmented cache would have no effect on the access time of the prediction entries. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the segmented cache. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

The advantage of a direct mapped cache is that there are more entries that can be used compared to a set-associated or fully associative cache of the same size (Stiles: Column 3 lines 64-67 continued to column 4 lines 1-10). Another advantage is

that the access time of the direct mapped cache is decreased because of the

assumption that the tag and look-up addresses match (Stiles: Column 4 lines 20-28).

Direct-mapped caches are also cheaper to use than their set or fully associative

counterparts due to fewer comparators needed to check for correct tags. The

advantages of increased capacity, decreased costs, and decreased access latency

would have motivated one of ordinary skill in the art at the time of the invention to

implement a direct-mapped branch prediction cache. Thus, it would have been obvious

to implement a direct-mapped branch prediction cache into the processor of Reinman

for the advantages of increased capacity, decreased costs, and decreased access

latency.

21.   As per claim 4:

The method as in claim 3, wherein an index of one of two sequential lines

corresponds to an entry on said first side of said cache, and an index of another of said

two sequential lines corresponds to an entry on said second side of said cache (Stiles:

Figure 9 element 155, column 15 lines 51-58)(It's inherent that in the segmented cache

two sequential instructions with an odd instruction address and an even instruction

address would be located in different segments of the cache.).

22.   As per claim 13:

Claim 13 essentially recites the same limitations of claim 3. Therefore, claim 13

is rejected for the same reasons as claim 3.

23.   As per claim 14:

Claim 14 essentially recites the same limitations of claim 4. Therefore, claim 14

is rejected for the same reasons as claim 4.

24.   As per claim 21:

Claim 21 essentially recites the same limitations of claim 3. Therefore, claim 21

is rejected for the same reasons as claim 3.

25.   As per claim 22:

Claim 22 essentially recites the same limitations of claim 3. Therefore, claim 22

is rejected for the same reasons as claim 3.

Response to Arguments

26.   The arguments presented by Applicant in the response, received on 8/18/2006

are partially considered persuasive.

27.   Applicant argues "Reinman failed to teach generating branch predictions for two

sequential lines in parallel during a prediction period."

This argument is found to be persuasive for the following reason. The examiner

agrees that Reinman failed to teach this limitation. However, a new ground of rejection

has been given to reject the added limitation.

28.   Applicant argues "Any combination of Reinman, Stiles, and Giacalone failed to

teach generating branch predictions for two sequential lines in parallel during a

prediction period" for claims 1, 12, and 20.

This argument is not found to be persuasive for the following reason. Giacalone is cited as teaching this limitation. The branch predictor of Giacalone is capable of making multiple branch predictions in parallel for multiple instructions.

29.   Applicant argues "Totsuka and Parady failed to teach generating branch predictions for two sequential lines in parallel during a prediction period" for claims 1, 12, and 20.

This argument is found to be persuasive for the following reason. The examiner agrees that these references failed to teach this limitation. Thus the rejections have been withdrawn and a new ground of rejection has been given for dependent claims 11 and 16.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

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